REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

The drawings were objected to for informalities. The specification was objected to for informalities. Claims 1, 2, 6, and 7 were objected to informalities. Claims 1-9 were rejected under 35 U.S.C. § 112, second paragraph. Claims 4 and 9 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1-11 were rejected under 35 U.S.C. § 102(b) as anticipated by the publication "A Core Generator For Fully Synthesizable And Highly Parameterizable Risc-Cores For System-On-Chip Designs" to Berekovic et al. (herein "Berekovic").

Addressing first the objection to the drawings, those objections are traversed by the present response.

Paragraph 3 of the Office Action objects to Figure 19 indicating that Figure 19 should be designated as "Prior Art". However, in that respect applicants note Figure 19 is clearly noted in the present specification as another embodiment of the present invention, see specifically the present specification at page 5, lines 31-33 and page 45, line 32 to page 46, line 3. Thus, Figure 19 is believed to be proper as originally presented without the label "Prior Art".

With respect to the objection of Figures 1, 6, 8, and 10, that objection is traversed by the present response.

Figures 1, 6, 8, and 10 were objected to as not utilizing the same terminology with respect to block 3 as in the specification. In response to that objection the specification is amended by the present response to now refer to element 3 as "user defined module/user defined command storage unit". Thus, the specification is now consistent with the labeling of element 3 in Figures 1, 6, 8, and 10.

With respect to the objections to the specification in paragraph 5 of the Office Action, the specification now updates the status of the parent application and incorporates the amendment noted at page 8, line 20. With respect to the objections noted at page 2, lines 14, 16 and page 4, line 2, applicants believe the specification was already proper in that regard. That is, applicants' version of the specification appears to recite the proper terms, and thus the specification at the above-noted portions and pages are believed to be proper.

With respect to the objection to claims 1, 2, 6, and 7, claims 1 and 6 are amended by the present response to now consistently refer to a "processor core", to provide clear antecedent basis for all terms. With respect to claims 2 and 7, those claims refer to plural "option instructions", and thus the term "include" is believed to be proper in those claims.

Addressing now the rejection of claims 1-9 under 35 U.S.C. § 112, second paragraph, that rejection is traversed by the present response.

Each of independent claims 1 and 6 now clarifies the selecting operations being "from given candidates". The amendment to claims 1 and 6 are believed to address the objections thereto under 35 U.S.C. § 112, second paragraph.

Addressing now the rejection of claims 4 and 9 under 35 U.S.C. § 112, second paragraph, those claims now clarify that the RTL templates are "accessible by the processor core" to clarify the language therein. Thus, claims 4 and 9 are believed to be in full compliance with all requirements under 35 U.S.C. § 112, second paragraph.

Addressing now the rejection of claims 1-11 under 35 U.S.C. § 102(b) as anticipated by Berekovic, that rejection is traversed by the present response.

The outstanding rejection cites Berekovic in Figure 1 to disclose operations of selecting a cache size, and selecting a data memory based on the Instruction RAM and the Data RAM shown in Figure 1. However, applicants respectfully submit Berekovic discloses that the cache memory, the Instruction RAM, and the Data RAM do not have the same way

of changing their sizes. The size change of the Instruction RAM and the Data RAM in Berekovic is performed only by fluctuating the number of cells that store data. In the case of the cache memory, not only a cell that stores data but a tag that stores data make a size of the cache memory changeable.

In contrast to Berekovic, in the claims the cache memory, instruction memory size, data memory size, and at least one of the plurality of option instructions are selected from given candidates.

The applicants of the present invention recognized that a cache memory is one of the important elements that can influence performance of a processor, and making cache size variable can lead to more optimal processor composition for applications to be processed. Thereby, in independent claims 1 and 6 a cache memory is selectable from given candidates. Such features are not taught or suggested in Berekovic.

Moreover, the applicants of the present invention also recognized that it is becoming common that two or more processors may appear in one chip in an on-chip system, which are becoming more large-scale in recent years, and that are increasingly desired to perform complicated processings with great amounts of data at high speed. The claimed invention can respond to such multi-processor compositions and can be applicable to such large-scale designs and can provide a more practical chip design.

In that respect, applicants also note independent claim 10 now further recites "preparing a configuration specifying a file including information concerning a multi-processor configuration". Such feature as clarified in independent claim 10 is also believed to be neither taught nor suggested by the applied art to Berekovic.

In such ways, applicants respectfully submit each of independent claims 1, 6, and 10, and the claims dependent therefrom, recite features neither taught nor suggested by

Berekovic. Thus, the claims as currently written are believed to distinguish over the applied art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870
Surinder Sachar
Registration No. 34,423

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)
EHK/SS:aif
I:\ATTY\SNS\24'S\240541\240541US-AM.DOC